REMARKS

The Office Action dated April 17, 2008 indicated that claims 4-10 would be allowable upon rewriting to include limitations of the base and intervening claims, and that claims 1-3 and 11-12 stand rejected under 35 U.S.C.§102(e) over Jacobson (U.S. Patent No. 6,499,124). Applicant fully traverses the rejections; Applicant further does not acquiesce to any rejection or averment in this Office Action unless Applicant expressly indicates otherwise.

The Section 102(e) rejections are improper because the Office Action has misconstrued the disclosure in the cited '124 reference, which fails to provide correspondence to the claimed invention. Specifically, the cited portions of the '124 reference do not provide correspondence to claim limitations directed to blocking an update signal for controlling the capture of a bit pattern passed between registers, or to controlling an update signal in response to the bit pattern. The passage of test signals between cells in the '124 reference is either passed or blocked completely, is not dependent upon an update signal and is further not carried out in response to the test signals themselves. The '124 reference thus cannot correspond to the claimed invention. These issues are discussed in greater detail below, with specific reference to cited and other portions of the '124 reference, and specific limitations in the claimed invention.

Referring to limitations of independent claim 1 (and as relevant to limitations of independent claim 11), the Office Action has asserted that the '124 reference discloses a "first register," "second register" and "dedicated control circuitry" as claimed. However, the cited security circuit 650-A(1) in FIG. 8 of the '124 reference, which the Office Action has alleged as providing correspondence to the claimed "dedicated control circuitry," does not block any update signal and does not operate in response to a bit pattern captured by a second register as claimed. Referring to FIG. 8, the cited security circuit 650-A(1) is coupled to a node between a shift register flip-flop 620(1) and a parallel latch 630(1), via conductive segment 625(1). The security circuit 650-A(1) functions to either pass or block a test data out (TDO) signal from passing between BSR cells in response to a stored security code, where the passage of TDO signals between the BSR cells is not dependent upon any update signal (*see*, *e.g.*, columns 8:66-9:14 and column 10:58-64). The cited "update" signal in the cited '124 reference is provided from a TAP controller to the parallel latch 630,

independently from the security circuit 650-A(1), and is not used to control the passage of data between BSR cells (*see*, *e.g.*, FIG. 8 and column 8:23-26).

In view of the above, the cited security circuit 650-A(1) thus functions to block test data signals "during INTEST or other Boundary Scan procedures" as described at column 8:32-36, and does so in response to a stored security code. The '124 reference's approach to controlling or blocking the passage of test data signals is done independently of any update signal (*i.e.*, the data is either passed or blocked entirely), and independently from any bit pattern passed between the BSR cells. The cited '124 reference thus fails to correspond to the claimed "dedicated control circuitry" that is "responsive to the bit pattern" captured by a second register, and thus cannot operate in accordance with the claimed dedicated control circuitry for controlling an update signal in response to a bit pattern.

New claims 13-16 are also allowable over the cited references for the reasons stated above, as relevant to claim limitations that are directed to subject matter including a control circuit that controls an update signal in response to a bit pattern, for controlling the capture of the bit pattern at a register. Specifically regarding claim 13, the limitations are directed to subject matter from dependent claim 4 and the claims from which it depends, which has been indicated as allowable in the Office Action. New claims 14-16 are similarly directed to limitations indicated to be allowable, relating to claims 5 and 6. Support for these claims may be found, for example, in the original claims and in FIG. 1, FIG. 2 and corresponding discussion at paragraphs 0037-0042.

In view of the above, Applicant believes that each of the rejections/objections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

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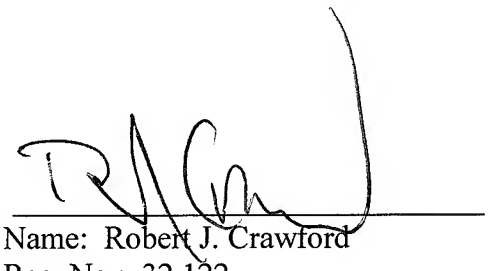
By: 

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